REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application, and for again correctly indicating as allowable the subject matter of dependent Claims 6-10, 14-19 and 22-24.

The independent claims have been amended to more clearly define the present invention over the cited prior art references. In particular, independent claims 4, 13 and 20 have been amended to better highlight that the memory is a shared memory between the interleaver and the deinterleaver. Support in the specification may be found on page 12, lines 7-10 and in FIG. 6, for example.

In view of the claim amendments and the arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates. As recited in amended independent Claim 4, for example, the device includes a channel coding/decoding stage comprising an interleaver, a deinterleaver, and a shared memory. More particularly, the shared memory has a minimum size based upon a maximum bit rate of the group of predetermined bit rates. A first memory space is assigned to the interleaver, and a second memory space is assigned to the deinterleaver. Moreover, a size of each of the first and second memory spaces is set as a function of the bit rate actually processed by the device.

Independent Claim 13 has been amended similar to independent Claim 4, but further recites that the shared memory is a shared random access memory, and that a Reed-Solomon coder/decoder is coupled to the interleaver and to the deinterleaver. Independent Claim 20 has also been amended similar to independent Claim 4, and is directed to a method for sending and receiving digital data and processing different bit rates.

II. The Claims Are Patentable

The Examiner rejected independent Claims 4, 13 and 20 based upon the Djokvic et al. patent in view of the Berlekamp et al. patent. The Djokovic et al. is directed to system for encoding DSL information streams having different latencies. The Examiner correctly acknowledges that this patent fails to teach a first memory space assigned to the interleaver and a second memory space assigned to the de-interleaver, sizes of which each are set as a function of the bit rate processed by the device.

The Examiner cited the Berlekamp et al. patent as providing this deficiency. In particular, the Examiner cited the Berlekamp et al. patent as disclosing an interleaving system that requires only one RAM for the interleaver and one additional RAM for the deinterleaver, each being a function of the bit rate.

The claimed invention, as recited in independent Claim 4 for example, has been amended to recite that the memory is shared between the interleaver and deinterleaver. The Djokvic et al. patent fails to disclose a memory shared by the interleaver and deinterleaver. The only reference to a

memory in the Djokovic et al. patent is in column 2, lines 38, 39 and 51, and this is with respect to the encoder.

In the Berlekamp et al. patent, FIG. 1 illustrates an encoder **14** with an interleaver **16** coupled thereto, and FIG. 2 illustrates a decoder with a deinterleaver **22** coupled thereto. A memory is disclosed in FIG. 5, but this is with respect to an interleaver. Like in the Djokovic et al. patent, the Berlekamp et al. patent fails to disclose a memory shared by the interleaver and deinterleaver.

In sharp contrast, independent Claim 4 has been amended to recite that the memory is a shared memory between the interleaver and deinterleaver. In other words, the shared memory is a common memory. For example, dependent Claim 12 recites that the memory is a dual-port memory. A dual-port memory allows multiple reads or writes to occur at the same time, or nearly the same time.

Amended independent Claim 4 further recites that the shared memory has a minimum size based upon a maximum bit rate of the group of predetermined bit rates. In the shared memory, a first memory space is assigned to the interleaver and a second memory space is assigned to the deinterleaver. A size of each of the first and second memory spaces is set as a function of the bit rate actually processed by the device. This advantageously allows the size of the memory required for the interleaving and deinterleaving implemented within the device to be reduced. The device may be a modem, for example.

Referring now to the claim recitation of the shared memory having a minimum size based upon a maximum bit rate of the group of predetermined bit rates, and the recitation that the size of each of the first and second memory spaces being

set as a function of the bit rate actually processed by the device, the Applicants submit that the Examiner mischaracterizes the teachings of the Berlekamp et al. patent.

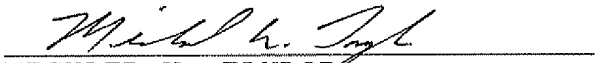
More particularly, the Berlekamp et al. patent fails to teach or suggest that a size of the interleaving and deinterleaving RAMs is set as a function of the bit rate actually processed by the device. The Berlekamp et al. patent provides no indication whatsoever as to the size or apportionment of the either the interleaver or deinterleaver RAMs. Moreover, the fact that data rates for reading/writing for the interleaver and deinterleaver are the same does not mean that their sizes are set as a function of the bit rate actually processed by the device. To hold otherwise would require the impermissible use of the claimed invention in hindsight as a template or roadmap to piece together the teachings of the prior art.

Accordingly, it is submitted that amended independent Claim 4 is patentable over the Djokvic et al. patent in view of the Berlekamp et al. patent. Amended independent Claims 13 and 20 are similar to amended independent Claim 4. Accordingly, amended independent Claim 13 and 20 are also patentable over the Djokvic et al. patent in view of the Berlekamp et al. patent. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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